IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of: Daniel CITRON
Serial No.: 10/721,316
Filed: November 25, 2003
For: REDUCING BUS WIDTH BY DATA COMPACTION

Group Art Unit: 2186
Examiner: Sheng-Jen Tsai

RULE 132 DECLARATION OF DANIEL CITRON

I, the undersigned, Daniel Citron of 20 Hamichon Street, Haifa, Israel, hereby declare as follows:

1. I am the Applicant in U.S. Patent Application No. 10/721,316 (hereinafter "the Application").

2. I have been employed as a professional in the field of computer systems and integrated circuit design for 15 years. I received a PhD degree in Computer Science from the Hebrew University of Jerusalem. I am currently employed as a computer scientist in the Code Optimization department of the Haifa Research Laboratory of IBM Corporation, in Haifa, Israel.

3. In 1995, together with Prof. Larry Rudolph, I published the article entitled "Creating a Wider Bus Using Caching Techniques" (hereinafter "the Article"), which has been cited against the Application.

4. The Article relates to compaction and caching techniques that may be used to solve problems that arise in "off-chip communications" because of the mismatch

between the wide internal data paths of microprocessors and the relatively smaller number of "pins per chip' that are available for off-chip communications (page 90, col. 1, last paragraph, continuing to top of col. 2). In this context, it should be understood that the term "pin" is universally used in the field of integrated circuits to refer to terminals for off-chip connections. This is the sense in which a worker in the field would have understood the term in 2003, as well.

5. The Article describes the use of a Bus-Expander for increasing effective bus bandwidth. It states explicitly that "the Bus-Expander... mediates between a device... and its connector" (page 91, col. 1, first paragraph in section 2, Description). Again, workers in the field would have understood the term "connector" as referring to connections between different chips (or even different circuit boards), and not to on-chip connections.

6. The Bus-Expander described in the Article uses a Look Up Table (LUT) to store a part of each device-word transmitted over the bus (typically the high-order bits). The effectiveness of the Bus-Expander is measured in terms of the number of "LUT hits," i.e., the number of times the high-order bits repeat themselves in successive device-words transmitted over the bus (page 91, col. 2 *et seq.*)

7. The Article describes simulation experiments that I performed in order to assess the effectiveness of the Bus-Expander (section 3, beginning at the bottom of col.

2 on page 92). It states explicitly that "the simulated system consists of a processor connected by a memory bus to a memory module... Bus-Expanders are situated between the processor and memory," which are connected by a 16-bit bus. Workers in the field (in both 1995 and in 2003) would have understood, based on the term "memory module" and the narrow (16-bit) bus width, that the memory is not located on the same chip as the processor.

8. In my experiments, I found that the LUT hit ratio of the Bus-Expander could be improved by the use of a cache on the processor chip for storing data and instructions (page 95, col. 1, section 3.2.2, first paragraph). I repeated the experiments using a number of different cache setups, including a second level cache (pages 95-97). In every case, however, the Bus-Expanders were used not within the processor chip, but rather between the cache on the chip and the memory module off the chip. For example, I stated in the article that "the effect of placing Bus-Expanders between a second level cache to memory was also tested" (page 97, col. 1, first paragraph, emphasis added). This arrangement is shown in Illustration 1 below.

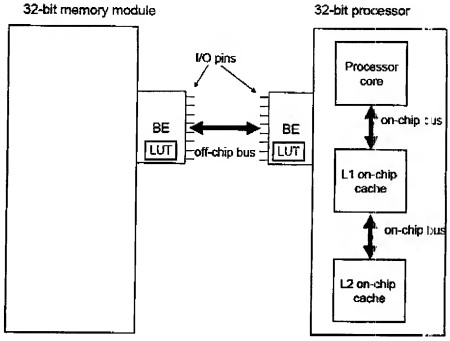

Illustration 1 - System described in the Article

9. By contrast, the Application relates exclusively and explicitly to the use of Bus-Expanders (BE) to transfer data within a chip (paragraph 0001). The independent claims in the Application, as they currently stand, relate to on-chip buses that are used to transfer data between a processing component, a L1 cache, and a L2 cache. This arrangement is shown in Fig. 3 of the Application, which is reproduced below as Illustration 2. The difference in where and how the Bus-Expanders are deployed is clearly demonstrated by the illustrations.

In Re: U.S.S.N. 10/721,316
Group Art Unit 2186
Rule 132 Declaration of Daniel Citron, cont'd

FIG. 3

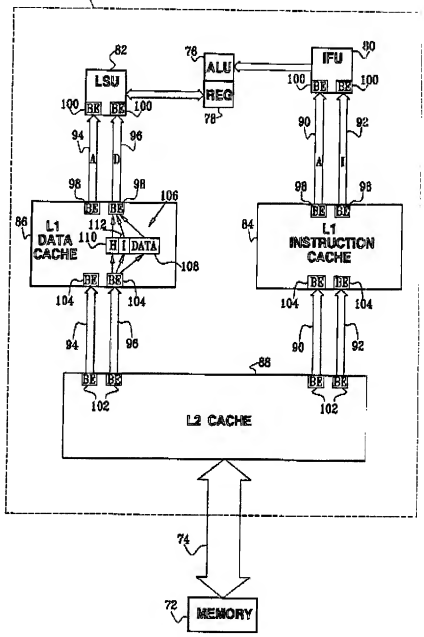

Illustration 2 – Fig. 3 from US 10/721,316

10. Furthermore, each of the Bus-Expanders in the

article has its own LUT, as shown above in Illustration 1. There is nothing in the article that would have suggested sharing one LUT between different bus expanders connected to the same cache, as is recited in the present claims. This sort of LUT sharing is exemplified in Illustration 2 above by entry 106, which is connected to both BE 98 and BE 104.

11. The points explained above demonstrate that a person of ordinary skill in the art in 2003 could not have understood the Article to teach or suggest the features of independent claims 1 and 14 as they currently stand in the Application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and conjecture are thought to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application of any patent issued thereon.

D. Citron

Daniel Citron, Citizen of Israel
20 Hatichon Street, Haifa, Israel
November 12, 2006